REMARKS

I. Status Of Claims

Claims 1-7 are pending in the present application. Claims 1, 4, and 5 were amended. Therefore, upon entry of this Amendment, Claims 1-7 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Claims 1 and 4 have been amended to place the claims in better method claim format.

II. Claim Rejections Under 35 U.S.C. § 103

Claims 1-7 stand rejected by the Examiner under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,043,133 to Jang et al. (hereinafter, "Jang") in view of U.S. Patent No. 5,420,133 to Hsu (hereinafter, "Hsu"). This rejection is respectfully traversed.

Claim 1 recites a method for the planarization of a semiconductor structure having a substrate, in which a plurality of substructures are provided. The substructures have a first substructure which has planar regions and first trench regions. The capacitor trenches (designated **DT**) shown in Figures 3A-3C of the present application are examples of the first trench regions recited by Claim 1. Claim 1 also recites that the substructures have a second substructure which comprises second trench regions. The

shallow trench isolation trenches (designated **STI**) shown in Figures 3A-3C of the present application are examples of the second trench regions recited by Claim 1. Claim 1 also recites that a layer to be planarized is applied over the semiconductor structure. The layer has corresponding first depressions above the first trench regions and corresponding second depressions above the second trench regions. Prior to planarizing the layer by a chemical mechanical polishing step, the layer is preplanarized by an etching step using a preplanarization mask. Claim 1 also recites by means of the preplanarization mask, provisioning a first region on the layer to be planarized above the first substructure, which region has a predetermined grid of masked and nonmasked sections. Further, Claim 1 recites arranging the masked and nonmasked sections in such a way that they respectively cover both first trench regions and planar regions. Claim 1 also recites creating a supporting structure for the chemical mechanical polishing step, which corresponds to the masked section of the grid, by the etching step using the preplanarization mask. Summarily, neither Jang nor Hsu, alone or in combination, teach or suggest each and every feature recited by Claim 1.

Jang discloses a method for the planarization of a semiconductor structure having a substrate in which a plurality of substructures are provided. In particular, Jang is directed to a method of forming a readable alignment marks on a wafer using a reverse tone photoresist etch mask **42B** and a chemical-mechanical polish process. (Jang, column 4, line 66, to column 5, line 3.) A shallow isolation trench (STI) photoresist mask **42A** is used to etch alignment area trenches **34** around alignment

marks **30** and to etch STI trenches **35** in device areas **14**. (Jang, column 5, lines 44-47.) Alignment area trenches **34** prevent over polishing of alignment marks **30**. (Jang, column 5, lines 47 and 48.) The semiconductor structure also includes active areas **37**. (Jang, column 5, lines 62-64.)

The Examiner contends that column 6, lines 64-66 of Jang discloses the Claim 1 recitation of the first trench regions being capacitor trenches and the second trench regions being STI trenches. (Official Action, page 3.) Referring to column 6, lines 64-66, of Jang, Jang describes simultaneously forming STI trenches **35** in device areas **14** while forming alignment area trenches **34** in an alignment mark trench area **18**. Applicants submit that alignment area trenches **34** are not capacitor trenches and are not part of the active area as required by Claim 1. Further, nowhere does Jang disclose or suggest capacitor trenches as required by Claim 1. Therefore, Jang does not disclose or suggest a semiconductor structure having a substrate in which a plurality of substructures are provided and in which one of the substructures has planar regions and capacitor trenches, as required by Claim 1.

The Examiner also contends that column 3, lines 32 and 33, and Figure 2C, of Jang discloses providing a patterned hard mask **22** on the surface of the substrate wherein the hard mask is open at the first and second trench regions as required by Claim 1. Referring to column 3, lines 32 and 33, of Jang, Jang discloses forming a polish stop layer **20 22** over a substrate **10**. Referring to Figure 2C, stop layer **20 22** has openings alignment area trenches **34** and STI trenches **35**. However, Jang does not

disclose the shape of active areas **37**. Therefore, there is no motivation for one of ordinary skill in the art to pattern stop layer **20 22** in the area corresponding to the active area. Therefore, Jang fails to disclose or suggest a patterned hard mask as required by Claim 1.

Hsu fails to overcome the significant shortcomings of Jang. In particular, Hsu fails to disclose or suggest a patterned mask being opened at the first and second trench regions as required by Claim 1. In addition, Hsu fails to disclose or suggest preplanarizing a layer to be planarized by an etching step using a preplanarization mask as required by Claim 1.

Hsu discloses a substrate with at least one hole, via or trench cut into the substrate. However, Hsu fails to disclose or suggest capacitor trenches and STI trenches as required by Claim 1. Further, Hsu fails to disclose or suggest a patterned mask being opened at the first and second trench regions as required by Claim 1. For this reason, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

Further, Hsu fails to disclose preplanarizing a layer to be planarized by an etching step using a preplanarization mask as required by Claim 1. In contrast, for example, Hsu discloses using removable templates for yielding the substrates with trenches as shown in Figure 7a. (Hsu, column 3, lines 59-63.) Hsu discloses using the template to form a structure in the substrate. There is no disclosure or suggestion of preplanarizing a layer as required by Claim 1. Therefore, for this additional reason, Claim 1 is believed

to be patentably distinguished over the combination of Jang and Hsu because the references do not disclose or suggest the presently claimed subject matter.

Claims 2-7 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 2-7.

Applicants respectfully submit that the teachings of Jang and Hsu, either alone or in combination, do not teach or suggest each and every feature of the present subject matter, and therefore that Claims 1-7 are not obvious in view of the Jang and Hsu. Applicants, therefore, respectfully request that the rejection of Claims 1-7 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

III. Conclusion

In light of the above remarks and amendments, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

DEPOSIT ACCOUNT

Although it is believed that no fee is due, the Commissioner is hereby authorized to charge any deficiencies of payment associated with the filing of this Response to Deposit Account No. **50-0426**.

Respectfully submitted,

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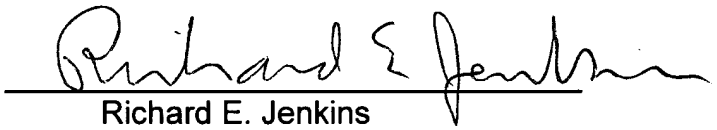
Date: July 22, 2005 By: 

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